1. A method of identifying one or more defective shift register latches in a scan chain, the method comprising:

electrically coupling a plurality of shift register latches into a series configuration so as to form a scan chain circuit, wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input;

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a shift clock pulse to the clock input of the second latch;

placing the scan chain circuit into an operating region; and

unloading the scan chain.

2. The method of claim 1, further comprising:

analyzing the scan chain results after the unloading step.

3. The method of claim 1, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all zeroes.

4. The method of claim 1, wherein the loading a scan test pattern into the scan chain circuit includes loading of all ones..

5. The method of claim 1, wherein the loading a scan test pattern into the scan chain circuit includes loading zero and ones.

6. The method of claim 5, wherein the loading a scan test pattern into the scan chain circuit includes loading an algorithmic scan test pattern.

7. The method of claim 1, wherein the unloading step comprises:

applying a scan clock pulse to the clock input of the first latch and a shift clock pulse to the input of the second latch;

measuring an output of the second latch against an expected response;

recording the result;

checking whether the scan chain has been completed; and

repeating the applying, the measuring and the recording steps until the scan chain is completed.

8. A method of identifying one or more defective shift register latches in a scan chain, the method comprising:

electrically coupling a plurality of shift register latches into a series configuration so as to form a scan chain circuit, wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input;

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a scan clock pulse to the clock input of the first latch;

placing the scan chain circuit into an operating region;

applying a shift clock pulse to the clock input of the second latch; and

unloading the scan chain.

9. The method of claim 8, further comprising:

analyzing the scan chain results after the unloading step.

10. The method of claim 8, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all zeroes.

11. The method of claim 8, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all ones.

12. The method of claim 8, wherein the loading a scan test pattern into the scan chain circuit includes loading zero and ones.

13. The method of claim 12, wherein the loading a scan test pattern into the scan chain circuit includes loading an algorithmic scan test pattern.

14. The method of claim 8, wherein the unloading step comprises:

applying a scan clock pulse to the clock input of the first latch and a shift clock pulse to the input of the second latch;

measuring an output of the second latch against an expected response;

recording the result;

checking whether the scan chain has been completed; and

repeating the applying, the measuring and the recording steps until the scan chain is completed.

15. A method of identifying one or more defective shift register latches in a scan chain, the method comprising:

electrically coupling a plurality of shift register latches into a series configuration so as to form a scan chain circuit, wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input;

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a scan clock pulse to the clock input of the first latch;

applying a shift clock pulse to the clock input of the second latch;

placing the scan chain circuit into an operating region; and

unloading the scan chain.

16. The method of claim 15, further comprising:

applying a shift clock pulse to the clock input of the second latch prior to unloading the latch.

17. The method of claim 15, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all zeroes.

18. The method of claim 15, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all ones.

19. The method of claim 15, wherein the loading a scan test pattern into the scan chain circuit includes loading zero and ones.

20. The method of claim 19, wherein the loading a scan test pattern into the scan chain circuit includes loading an algorithmic scan test pattern.

21. A computer program product containing programming instructions for identifying one or more defective shift register latches in a scan chain, wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input, the programming instructions comprising:

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a shift clock pulse to the clock input of the second latch;

placing the scan chain circuit into an operating region; and

unloading the scan chain.

22. A computer program product containing programming instructions for identifying one or more defective shift register latches in a scan chain, wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input, the programming instructions comprising:

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a scan lock pulse to the clock input of the first latch;

applying a shift clock pulse to the clock input of the second latch;

placing the scan chain circuit into an operating region; and

unloading the scan chain.